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10/707,647	12/30/2003	Hong-Ping Tsai	EMEP0063USA	1646

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EXAMINER
KAPLAN, HAL IRA

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 10/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,647	TSAI ET AL.	
	Examiner	Art Unit	
	Hal I. Kaplan	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on December 30, 2003. These drawings are accepted.

Claim Objections

2. Claims 1, 6-8, 14, 15, 17, 20, and 21 are objected to because of the following informalities: Claims 1, 6-8, 14, 15, 17, 20, and 21 contain the phrases "first power" and "second power". It appears these should be "first power source" and "second power source". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-7 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by the US patent of Savelli (6,133,777).

As to claim 1, Savelli, drawn to a selector circuit for the switching over of analog signals with amplitudes greater than that of the supply voltage, discloses a high power auto selecting circuit (3,4) comprising: a first transistor (3) where a first terminal of the first transistor (3) is electrically coupled to a first power (output of switch circuit 1), a second terminal of the first transistor (3) is electrically coupled to an output node (Vpp), and a gate of the first transistor (3) is electrically coupled to a second power (output of

switch circuit 2); and a second transistor (4) where a first terminal of the second transistor (4) is electrically coupled to the second power (output of switch circuit 2), a second terminal of the second transistor (4) is electrically coupled to the output node (Vpp), and a gate of the second transistor (4) is electrically coupled to the first power (output of switch circuit 1); wherein the high power auto selecting circuit selectively generates an output voltage according to a higher one of the voltages output by the first power and the second power automatically (see column 2, lines 43-52; column 2, line 57 through column 3, line 16; and the Figure; in the example of Savelli, one of the first and second voltages is always 0V and the other is always Vpp1 or Vpp2 (the high voltage selecting circuit 3,4 will work for any two voltages), wherein the first power (Vpp1) and the second power (Vpp2) are external power sources; of these, the output of the high voltage selecting circuit (3,4) is always Vpp1 or Vpp2, either of which is higher than 0V; switch circuits 1 and 2 are not part of the high voltage selecting circuit).

As to claim 2, the first transistor (3) is a p-type MOS transistor and the first terminal of the first transistor is a source and the second terminal of the first transistor is a drain (see column 2, lines 43-47).

As to claim 3, the second transistor (4) is a p-type MOS transistor and the first terminal of the second transistor is a source and the second terminal of the second transistor is a drain (see column 2, lines 48-52).

As to claim 4, the first transistor (3) further comprises a well and the well is electrically coupled to the second terminal of the first transistor (3) (see column 2, lines 43-47 and the Figure).

As to claim 5, the second transistor (4) further comprises a well and the well is electrically coupled to the second terminal of the second transistor (4) (see column 2, lines 48-52 and the Figure).

As to claim 6, when an absolute value of a difference between the voltages output by the first power (output of switch circuit 1) and the second power (output of switch circuit 2) is larger than a threshold voltage of the first and second transistors (3,4), the output voltage (Vpp) is substantially a higher voltage output by the first power and the second power (see column 2, lines 53-56; in the example of Savelli, since the control signals are complementary, one of the inputs to the high voltage selecting circuit in the example of Savelli will always be 0V and the other will always be either Vpp1 or Vpp2; if the absolute value of the other (Vpp1 or Vpp2) voltage is greater than the threshold voltage of the transistors (3,4), the absolute value of the difference between the other voltage and 0V will therefore be equal to the absolute value of the other voltage and greater than the threshold voltage of the transistors (3,4)).

As to claim 7, when an absolute value of the other voltage (Vpp1 or Vpp2) is smaller than the threshold voltage of the first and second transistors, the absolute value of the difference between the other voltage and 0V will be equal to the absolute value of the other voltage and therefore less than the threshold voltage of the transistors (3,4), causing both transistors (3,4) to be in the off state, and the output voltage will be the other voltage (which is higher than 0V) less a junction voltage between first terminal of its respective transistor (3,4) and the well of its respective transistor (3,4).

As to claim 20, the voltages output by the first power (Vpp1) and the second power (Vpp2) are not related to one another in any way.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 8, 10-16, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Savelli in view of the US patent of Seki (5,122,692).

As to claim 8, Savelli discloses all of the claimed features, as set forth above, except for a level shifting module and a selecting switch module. Seki, drawn to a high speed level conversion circuit including a switch circuit, discloses a level shifting module (41) for inputting a voltage (V_{CC}) as a power supply of the level shifting module (41), for performing level shift on a first control signal (IN) according to the power supply voltage (V_{CC}) (see column 3, lines 41-54 and Figure 4); and a selecting switch module (42) electrically coupled to the level shifting module (41), for selectively outputting the voltage output by the first power (OUT) or the voltage output by the second power (OUT') according the level-shifted first control signal (C) (see column 3, line 55 through column 4, line 28 and Figure 4). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to connect the high voltage selecting module of Savelli to the level shifting module and selecting switch module of Seki, with the output voltage (Vpp) of the high voltage selecting module of Savelli as the power supply voltage (V_{CC}) of the circuit of Seki, in order to minimize power consumption and easily generate the output voltages.

As to claims 10-15 and 21, Savelli discloses the claimed subject matter, as set forth above.

As to claim 16, the level shifting module (41) of Savelli further performs level shift on a second control signal (IN') according to the power supply voltage and the second

control signal (IN') is complementary to the first control signal (IN) (see column 3, lines 46-48).

9. Claims 17-19 rejected under 35 U.S.C. 103(a) as being unpatentable over Savelli and Seki, and further in view of admitted prior art (admission).

As to claim 17, Savelli in view of Seki disclose all of the claimed features, as set forth above, except for the selecting switch module further comprising: a third transistor where a first terminal of the third transistor is electrically coupled to a first power, a second terminal of the third transistor is electrically coupled to a supply node, and the gate of the third transistor is electrically coupled to a level-shifted first control signal; and a fourth transistor where a first terminal of the fourth transistor is electrically coupled to a second power, a second terminal of the fourth transistor is electrically coupled to the same supply node as the second terminal of the third transistor, and the gate of the fourth transistor is electrically coupled to a level-shifted second control signal.

Admitted prior art discloses a selecting switch module further comprising: a third transistor (20) where a first terminal of the third transistor (20) is electrically coupled to a first power (V_{PP}), a second terminal of the third transistor (20) is electrically coupled to a supply node (V_{PS}), and the gate of the third transistor (20) is electrically coupled to a level-shifted first control signal (ENVPPHV); and a fourth transistor (22) where a first terminal of the fourth transistor (22) is electrically coupled to a second power (V_{DD}), a second terminal of the fourth transistor (22) is electrically coupled to the same supply node (V_{PS}) as the second terminal of the third transistor (20), and the gate of the fourth transistor (22)is electrically coupled to a level-shifted second control signal (ENVDDHV).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to connect the output (C) of the level shifting module of the circuit of Savelli in view of Seki to the admitted prior art selecting switch module, in order to provide a sufficiently high signal to the selecting switch module to increase reliability.

As to claim 18, the third transistor (Q_{P2}) of Savelli in view of Seki is a p-type MOS transistor and the first terminal of the third transistor (Q_{P2}) is a source and the second terminal of the third transistor (Q_{P2}) is a drain (see Seki, column 3, line 58).

As to claim 19, the fourth transistor (Q_{P1}) of Savelli in view of Seki is a p-type MOS transistor and the first terminal of the fourth transistor (Q_{P1}) is a source and the second terminal of the fourth transistor (Q_{P1}) is a drain (see Seki, column 3, lines 56-57).

Response to Arguments

10. Applicant's arguments, see Remarks, filed August 23, 2006, with respect to the objections have been fully considered and are persuasive. The objections have been withdrawn.

11. As to claims 1-19, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., that the first and second transistors are connected directly to the first and second external power sources) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The only power sources disclosed by Savelli are the

two external power sources, so the first and second transistors must receive power from the two external power sources. In addition, the layout and connection of transistors 3 and 4 can be connected directly to any two power sources, not only the outputs of switching circuits. The switching circuits ensure that the gate voltage of the pmos transistor connected to the larger voltage is 0V, which simply ensures that the voltage output by the greater of the first and second power sources will be generated at the output of the circuit, even if the difference between the voltages output by the two power sources is very small. If there were no switching circuits, this would still be the case, except the gate voltage of the transistor connected to the larger voltage will not be 0V (but will still be high enough to turn the transistor off while the other transistor will be turned on). Savelli was cited for first and second transistors 3 and 4 being connected to different external power sources, and the greater voltage being output, not for the use of switching circuits.

12. As to claims 20 and 21, the layout and connection of transistors 3 and 4 of Savelli will work with two power sources that are not related to one another in any way, as set forth above.

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hal I. Kaplan whose telephone number is 571-272-8587. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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